AMENDMENTS TO THE SPECIFICATION

Please amend the specification by rewriting the following paragraphs as demonstrated below in marked up form.

Please amend the paragraph beginning on page 2, line 10, with the following paragraph:

Summarizing the problems to be solved by the invention, the above power amplifier does not suffer from any problems at room temperature, but if the ambient temperature changes, there is the problem that the bias current of the power amplifier changes greatly from the setting at room temperature especially at ~~the~~ low temperature or high temperature. As a result, the linearity of the power amplifier remarkably deteriorates.

Please amend the paragraph beginning on page 9, line 16, with the following paragraph:

The power amplifier 10 has, as shown in FIG. 2, ~~an~~ a FET (field effect transistor) 11, a bias voltage supply terminal 12 supplied with a plus voltage Vgg, a power source voltage supply terminal 13 supplied with a power source voltage Vdd, a ground potential (reference potential) GND, a first resistance element R11, and a second resistance element R12 with a temperature coefficient smaller than that of the first resistance element R11.

Please amend the paragraph beginning on page 9, line 25 and continuing onto page 10, with the following paragraph:

A first terminal of the first resistance element R11 and a first terminal of the second resistance element R12 are connected and the connection point ND11 is connected to a gate terminal G of the FET 11. A second terminal of the first resistance element R11 is connected to the bias voltage supply terminal 12, and a second terminal of the second resistance element R12 is connected to the ground potential GND. A drain terminal D of the ~~TFT~~ FET 11 is connected to the power source voltage supply terminal 13, and a source terminal S is connected to the ground potential GND. The FET 11 and the first resistance element R11 are semiconductor devices formed on the same semiconductor substrate 14.

Please amend the paragraph beginning on page 11, line 13, with the following paragraph:

The power amplifier 20 has, as shown in FIG. 3, ~~an~~ a FET (field effect transistor) 21, a bias voltage supply terminal 22 supplied with a plus bias voltage Vgg, a power source voltage supply terminal 23 supplied with a power source voltage Vdd, a ground potential (reference potential) GND, a first resistance element R21, a second resistance element R22, and a third resistance element R23 with a temperature coefficient smaller than those of the first resistance element R21 and the second resistance element R22.

Please amend the paragraph beginning on page 12, line 14 and continuing onto page 13, with the following paragraph:

In this power amplifier 20, since the temperature coefficients of resistance of the first resistance element R21 and the second resistance element R22 at the bias voltage supply side are larger than that of the third resistance element R23 at the ground side, the voltages supplied to the gate terminal G of the FET 21 change in accordance with changes of the ambient temperature. Due to this, the power amplifier 20 is supplied with the optimum bias voltage in accordance with each temperature. As a result, it is possible to prevent the deterioration of the basic characteristics, especially the linearity. Further, since the FET 21, the first resistance element R21, and the second resistance element R22 are formed on the same semiconductor substrate 24, it is possible to reduce the number of ~~the~~ parts in comparison with bias circuits constituted by so-called chip resistors. Accordingly, there is the advantage that the size of the power amplifier can be reduced.

Please amend the paragraph beginning on page 13, line 17 and continuing onto page 14, with the following paragraph:

The power amplifier 30 has, as shown in FIG. 4, ~~an~~ a FET (field effect transistor) 31, a bias voltage supply terminal 32 supplied with a plus bias voltage Vgg, a power source voltage supply terminal 33 supplied with a power source voltage Vdd, a ground potential (reference potential) GND, a first resistance element R31, a second resistance element R32 with a temperature coefficient smaller than that of the first resistance element R31, and a third resistance element R33 with a temperature coefficient smaller than that of the first resistance element R31.

Please amend the paragraph beginning on page 14, line 18 and continuing onto page 15, with the following paragraph:

In this power amplifier 30, since the temperature coefficient of resistance of the first resistance element R31 at the bias voltage supply side is larger than those of the second resistance element R32 and the third resistance element R33 at the ground side, the voltages supplied to the gate terminal G of the FET31 change in accordance with changes of the ambient temperature. Due to this, the power amplifier 30 is supplied with the optimum bias voltage in accordance with each temperature. As a result, it is possible to prevent the deterioration of the basic characteristics, especially the linearity. Further, since the FET 31 and the first resistance element R31 are formed on the same semiconductor substrate 34, it is possible to reduce the number of ~~the~~ parts in comparison with bias circuits constituted by so-called chip resistors. Accordingly, there is the advantage that the size of the power amplifier can be reduced.

Please amend the paragraph beginning on page 15, line 24 and continuing onto page 16, with the following paragraph:

The power amplifier 40 has a plurality of FETs, for example the two FETs 41 and ~~FET~~ 42 in this embodiment. The power amplifier 40 has, as shown in FIG. 5, a bias circuit 43 of the FET 41, a bias circuit 44 of the FET 42, an input matching circuit 45 connected between a connection point ND41 connected to a gate terminal G of the FET 41 of the bias circuit 43 and an input terminal TIN, an inter-stage matching circuit 46 connected to a drain terminal D of the FET 41 and a connection point ND42 connected to a gate terminal G of the FET 42 of the bias circuit 44, and an output matching circuit 47 connected between a drain terminal D of the FET 42 and an output terminal TOUT.

Please amend the paragraph beginning on page 16, line 12, with the following paragraph:

In the bias circuit 43, elements R41 and R42 are connected in series between a bias voltage supply terminal 48 supplied with a plus bias voltage Vgg and the ground potential GND, and the connection point ND41 of resistance elements R41 and R42 is connected to the gate terminal G of

the FET 41. The drain terminal D of the ~~TFT~~ FET 41 is connected to a supply terminal 49 of the power source voltage Vdd, and a source terminal S of the FET 41 is grounded.